AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (original) A semiconductor package comprising:

at least one plate-like mount;

a semiconductor chip having at least one electrode formed on a top surface thereof, and mounted on said plate-like mount such that a bottom surface of said semiconductor chip is in contact with said plate-like mount;

at least one lead element having an outer portion arranged to be flush with said plate-like mount, and an inner portion deformed and shaped to overhang said semiconductor chip such that an inner end of said lead element is spaced apart from the top surface of said semiconductor chip;

a bonding-wire element bonded at ends thereof to the electrode of said semiconductor chip and the inner end of said lead element; and

an enveloper sealing and encapsulating said plate-like mount, said semiconductor chip, the inner portion of said lead element, and said bonding-wire element.

2. (currently amended) A semiconductor package as set forth in claim 1, wherein said electrode is defined as a first

electrode, and said lead element is defined as a first lead element,

said semiconductor chip further having a second electrode formed on the top surface thereof,

said semiconductor package further comprising a second lead element having an outer portion arranged to be flush with said plate-like mount, and an inner portion deformed and shaped to overhang said semiconductor chip such that an inner end of said second lead element is directly and electrically connected to the second electrode of said semiconductor chip, using an electrically conductive paste.

3. (original) A semiconductor package as set forth in claim 2, wherein said semiconductor chip is constructed as a MOSFET chip having a drain electrode formed on a bottom surface thereof and electrically connected to said plate-like mount, with said respective first and second electrodes being defined as a source electrode and a gate electrode, and said plate-like mount has at least one lead element extending therefrom.

4. (original) A semiconductor package as set forth in claim 3, wherein said MOSFET chip is formed as a high power type, and the source electrode has a larger area than that of said gate electrode.

5. (original) A semiconductor package as set forth in claim 4, wherein the sealing and capsulation of said plate-like

mount in said enveloper is carried out such that a bottom surface of said plate-like mount is exposed to outside.

6. (original) A semiconductor package as set forth in claim 1, wherein said electrode is defined as a first electrode, and said lead element is defined as a first lead element,

said semiconductor chip further having a second electrode formed on the top surface thereof,

said semiconductor package further comprising: a second lead element having an outer portion arranged to be flush with said plate-like mount, and an inner portion deformed and shaped to overhang said semiconductor chip such that an inner end of said second lead element is spaced apart from the top surface of said semiconductor chip; and at least one bonding-wire element bonded at ends thereof to the electrode of said semiconductor chip and the inner end of said second lead element.

7. (original) A semiconductor package as set forth in claim 6, wherein said semiconductor chip is constructed as a MOSFET chip having a drain electrode formed on a bottom surface thereof and electrically connected to said plate-like mount, with said respective first and second electrodes being defined as a source electrode and a gate electrode, and said plate-like mount has at least one lead element extending therefrom.

8. (original) A semiconductor package as set forth in claim 7, wherein said MOSFET chip is formed as a high power type,

and the source electrode has a larger area than that of said gate electrode.

9. (original) A semiconductor package as set forth in claim 8, wherein the sealing and capsulation of said plate-like mount in said enveloper is carried out such that a bottom surface of said plate-like mount is exposed to outside.

10. (original) A semiconductor package as set forth in claim 1, wherein said semiconductor chip has another electrode formed on a bottom surface thereof and electrically connected to said plate-like mount, and said plate-like mount has at least one lead element extending therefrom.

11. (original) A semiconductor package as set forth in claim 10, said semiconductor chip is constructed as a diode chip, with one of the electrodes formed on the top and bottom surfaces of said semiconductor chip being defined as an anode electrode, the remaining electrode being defined as a cathode electrode.

12. (original) A semiconductor package as set forth in claim 11, wherein said diode chip is formed as a high power type.

13. (original) A semiconductor package as set forth in claim 12, wherein the sealing and capsulation of said plate-like mount in said enveloper is carried out such that a bottom surface of said plate-like mount is exposed to outside.

14. (original) A semiconductor package as set forth in claim 1, wherein said electrode is defined as a first electrode, and said lead element is defined as a first lead element,

said semiconductor chip further having a second electrode formed on the top surface thereof,

said semiconductor package further comprising: a second lead element having an outer portion arranged to be flush with said plate-like mount, and an inner portion deformed and shaped to overhang said semiconductor chip such that an inner end of said second lead element is spaced apart from the top surface of said semiconductor chip; and a bonding-wire element bonded at ends thereof to the electrode of said semiconductor chip and the inner end of said second lead element.

15. (original) A semiconductor package as set forth in claim 14, said semiconductor chip is constructed as a diode chip, with one of the electrodes formed on the top surface of said semiconductor chip being defined as an anode electrode, the remaining electrode being defined as a cathode electrode.

16. (original) A semiconductor package as set forth in claim 15, wherein said diode chip is formed as a high power type.

17. (original) A semiconductor package as set forth in claim 16, wherein the sealing and capsulation of said plate-like mount in said enveloper is carried out such that a bottom surface of said plate-like mount is exposed to outside.

18-22. (canceled)

23. (new) A semiconductor package comprising:

a planar mounting element;

a semiconductor chip having at least one electrode formed on a top surface thereof, said semiconductor chip being mounted on said planar mounting element such that a bottom surface of said semiconductor chip is in contact with said planar mounting element;

a first lead element having an outer portion arranged to be flush with said planar mounting element, and an inner portion deformed and shaped to overlap said semiconductor chip such that an inner end of said lead element is spaced apart from and directly overlies the top surface of said semiconductor chip;

a bonding-wire bonded at ends thereof to the electrode of said semiconductor chip and the inner end of said lead element; and

an enveloper sealing and encapsulating said planar mounting element, said semiconductor chip, the inner portion of said lead element, and said bonding-wire.

24. (new) A semiconductor package comprising:

a planar mounting element;

a semiconductor chip having first and second electrodes formed on a top surface thereof, said semiconductor chip being mounted on said planar mounting element such that a bottom surface of said semiconductor chip is in contact with said planar mounting element, said first and second electrodes being defined respectively as a source electrode and a drain electrode, the

bottom surface of said semiconductor chip being defined as a drain electrode;

a first lead element having an outer portion arranged to be flush with said planar mounting element, and an inner portion deformed and shaped to overlap said semiconductor chip such that an inner end of said lead element is spaced apart from and overlies the top surface of said semiconductor chip;

a bonding-wire bonded at ends thereof to the electrode of said semiconductor chip and the inner end of said lead element;

a second lead element having an outer portion arranged to be flush with said planar mounting element, and an inner portion deformed and shaped to overlap said semiconductor chip such that an inner end of said second lead element is directly and electrically connected to the second electrode of said semiconductor chip, using an electrically conductive paste; and

an enveloper sealing and encapsulating said planar mounting element, said semiconductor chip, the inner portions of said first and second lead elements, and said bonding-wire.